Tehnici de Proiectare CIEM . CIEM pe o Placa de Circuit Imprimat (Printed Circuit Board - PCB) : Introducere .Mecanisme de Cuplaj .

1. Introducere

Sunt discutate subiectele urmatoare:

(i) mecanismele de cuplare si problemele asociate cuplajelor : cuplaje datorita conductiei (e.g. datorate surselor de putere), cuplaje capacitive si inductive ;

(ii) arhitecturi si configuratii : utilizarea suprafetelor plane legate la pamint, ecranari (blindaje) locale, decuplarea surselor de putere, semnale terminale ;

(iii) IEM si circuitele digitale (numerice) : familii de circuite logice (TTL / NMOS / CMOS / si ECL) si caracteristicile acestora, sursele problemelor si susceptibilitati, "corectii" : semnale terminale, limitele de zgomot, impedante de circuit si de traseu, cresterea intervalului de timp, si configuratii de interconectare ;

(iv) IEM si circuitele analogice : surse de IEM, susceptibilitati, proiectare pentru eliminarea problemelor, efectul impedantei de circuit, utilizarea suprafetelor plane legate la pamint, blindaje (ecranari legate la pamint), trasee ecranate si inbunatatirea conexiunilor pe placa imprimata .

2. Mecanisme de Cuplaj

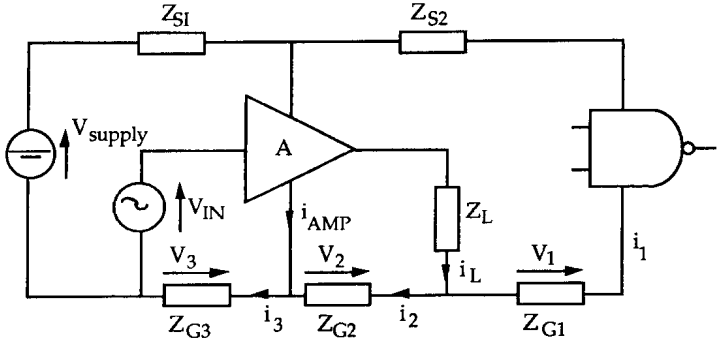
Propagarea Interferentei

prin Conductie		prin Radiatie	
Impedanta obisnuita (comuna)	**Frecvente joase** $d \ll l/(2p)$ $d \gg \frac{l}{2p}$	**Cimp Electric**	**Cimp Magnetic**
Linia de Transmisie	**Frecvente inalte** $d > l/(2p)$ $d \geq \frac{l}{2p}$	**Unda Electro-Magnetica**	

Mecanismele de Cuplaj

2.1. Cuplajul prin Imppedanta Comuna

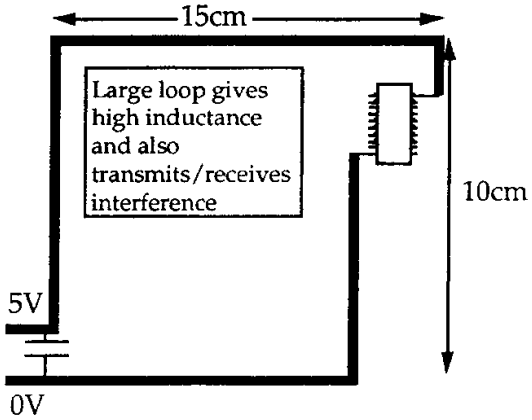
$$V_3 = Z_{G3}\, i_3 = Z_{G3}\,(i_1 + i_L + i_{AMP})$$



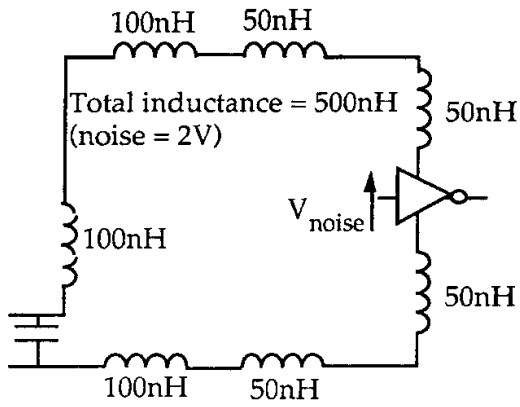
$V_3 = i_3\, Z_{G3} = (i_1 + i_L + i_{AMP})\, Z_{G3}$

Principiul Cuplarii prin intermediul Impedantei comune

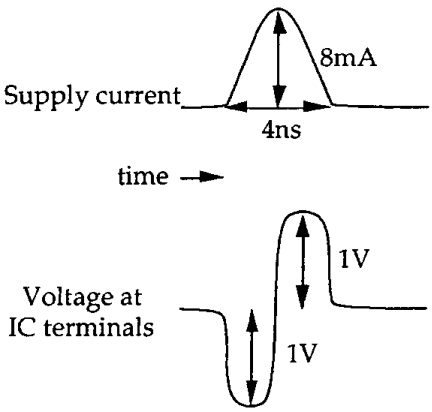
2.1.1. Optimizarea Aranjarii Conexiunilor (Cailor de Conductie)



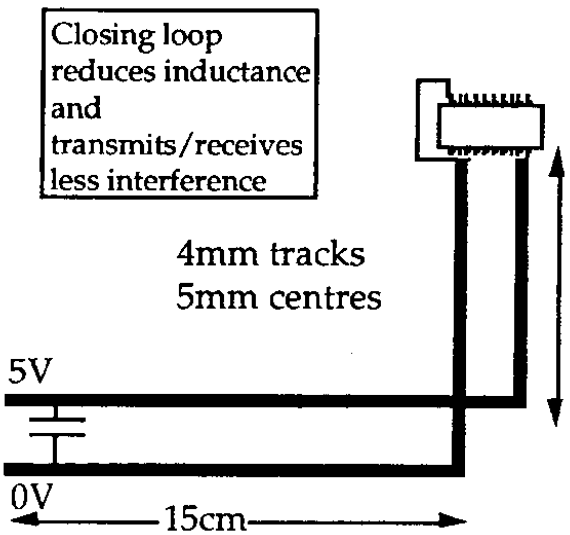
Configuratie de circuit inadecvata



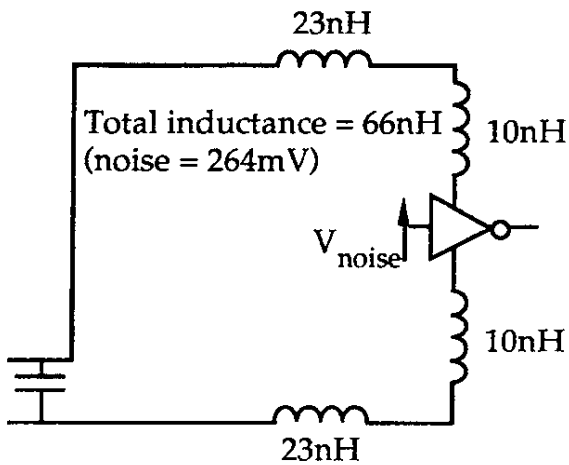
Circuitul echivalent pentru Configuratie de circuit inadecvata



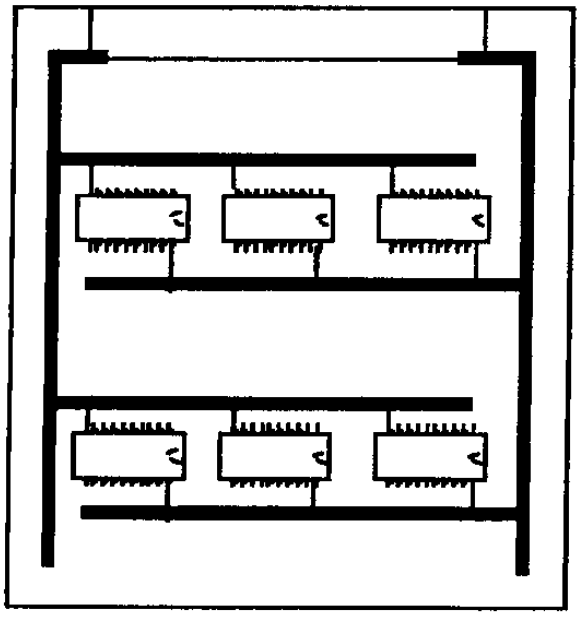
Curentul de sarcina si tensiunea de zgomot pe parcursul comutarii (comutatiei)



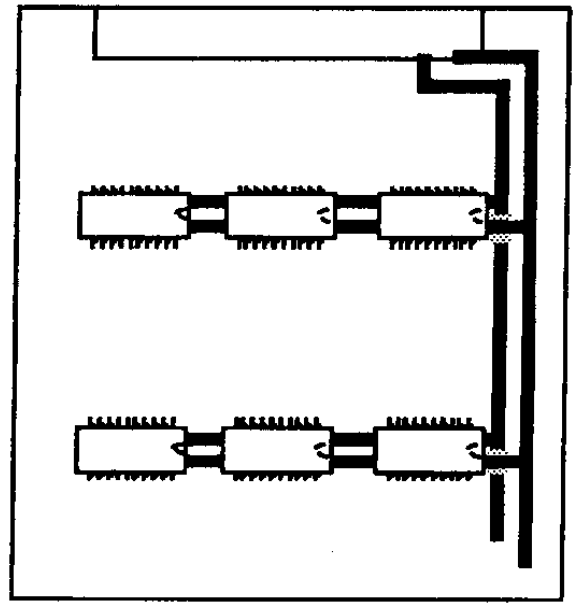
Configuratie de circuit imbunatatita



Circuitul echivalent pentru Configuratie de circuit imbunatatita

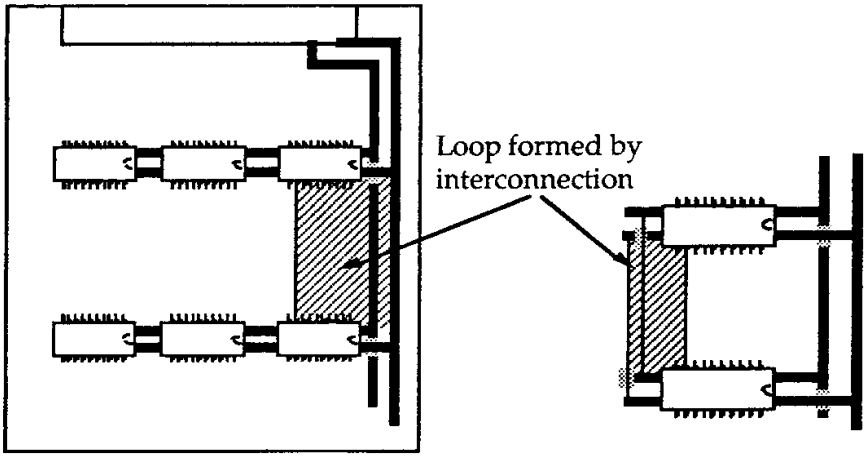


Poor layout



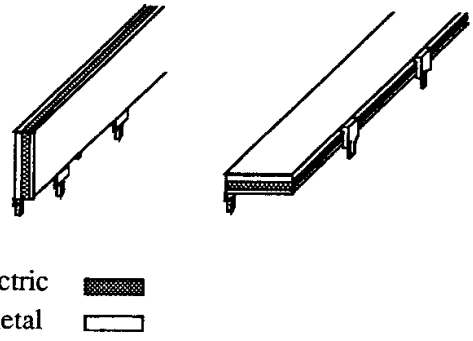
Improved layout

Conectarea corecta si incorecta a sursei de putere pentru intreaga placa imprimata



Efectul conectarii semnalelor si Grila de alimentare reduce domeniile buclelor de semnal

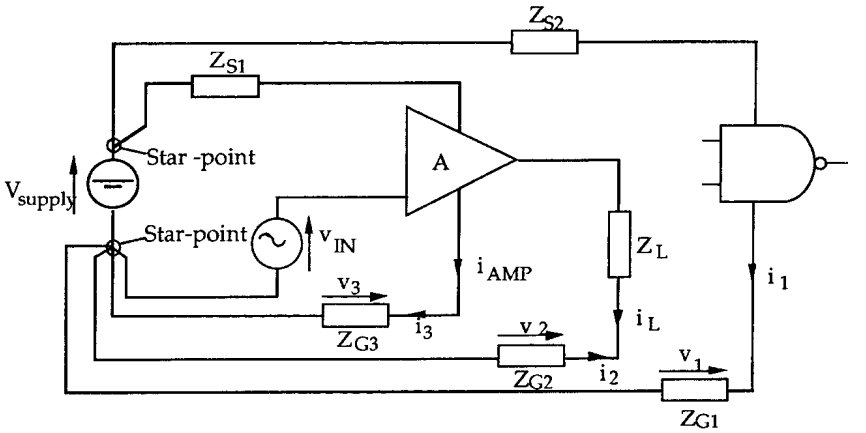
2.1.2. Conexiuni pentru surse de putere de joasa impedanta separate



Tipuri de Conectoare pentru sursa de putere

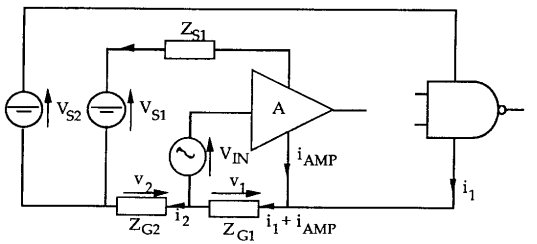
2.1.3. Suprafete pentru surse de putere

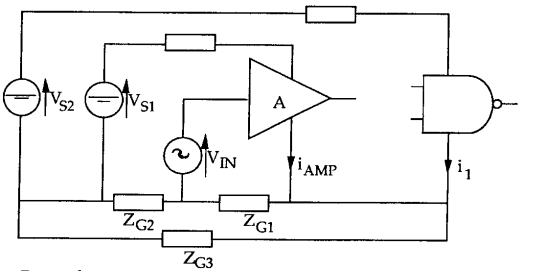
2.1.4. Conexiuni in stea



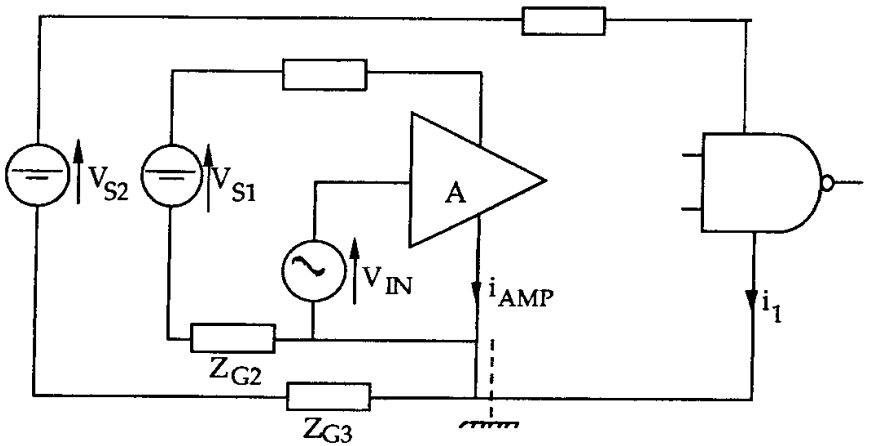
Reducerea cuplajului prin intermediul impedantei comune utilizind conexiunile in stea cu pamintare a surselor de putere

2.1.5. Surse de putere separate





Mod de conectare gresit **Mod de conectare corect dar nu foarte bun**

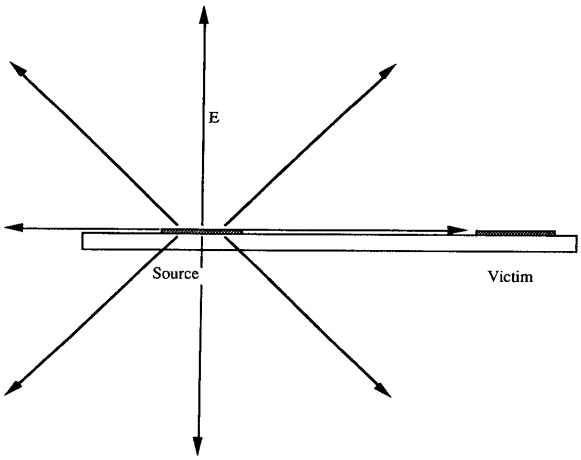


Mod de conectare optim

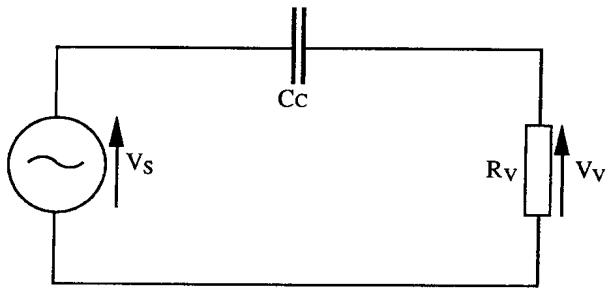
Utilizarea surselor de putere separate pentru a minimiza cuplajul dintre circuite

2.1.6. Concluzii

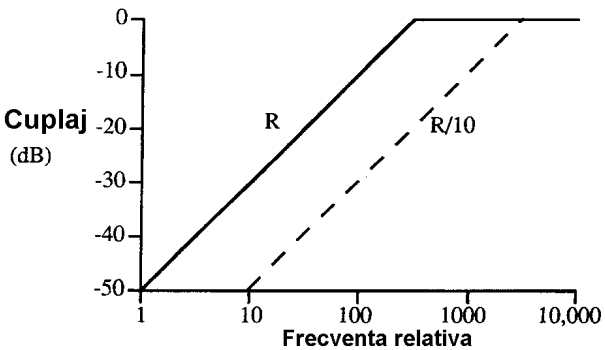
2.2. Cuplaj capacitiv



Cuplajul capacitiv dintre conductoare aflate foarte aproape



Circuitul echivalent pentru conductoare cuplate capacitiv considerind o victima cu sarcina rezistiva



Raspunsul in frecventa pentru conductoarele cuplate capacitiv cu sarcina (impedanta de sarcina) rezistiva

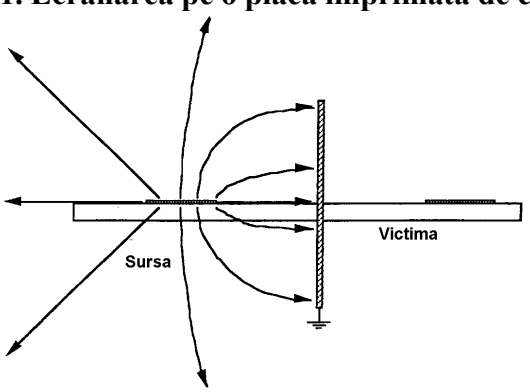
(1) $$I_V = C_C \frac{dV_{SV}}{dt}$$

(2) $$V_V = Z_V I_V$$

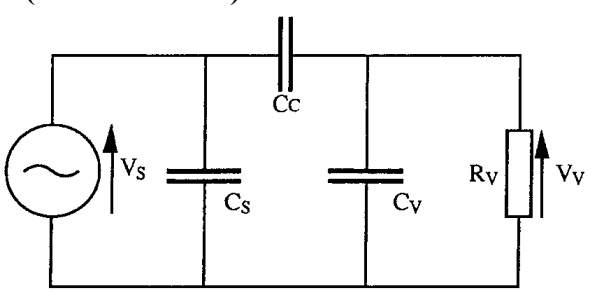
$$V_V = Z_V \cdot I_V$$

(3) $$\frac{V_V}{V_S} = \frac{jw\, C_C Z_V}{1 + jw\, C_C Z_V}$$

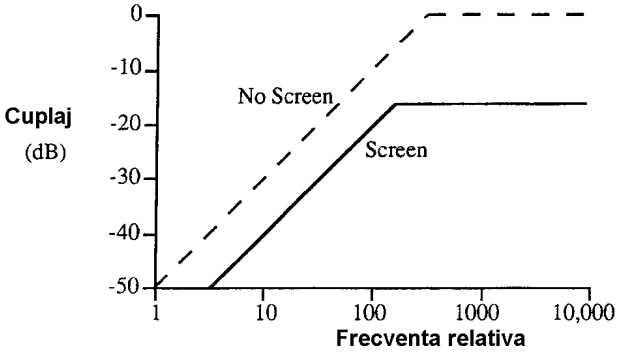
2.2.1. Ecranarea pe o placa imprimata de circuit (PIC sau PCB)



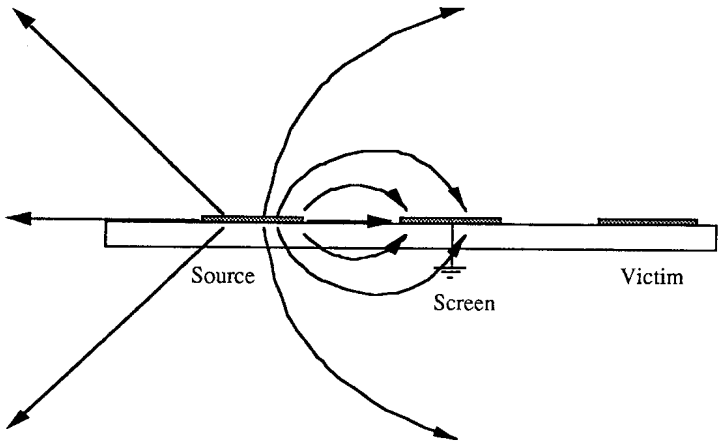
Un ecran reduce cimpul electric, datorat sursei, asupra victimei



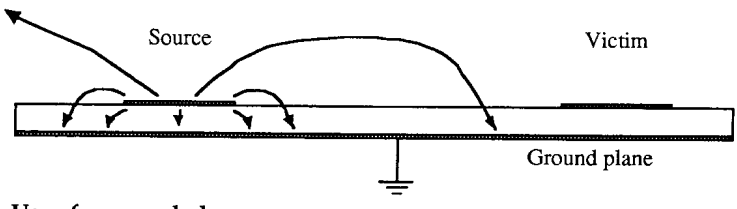
Circuitul echivalent pentru conductoare cuplate cu ecranare



Cuplajul pentru circuite ecranate in comparatie cu circuite neecranate



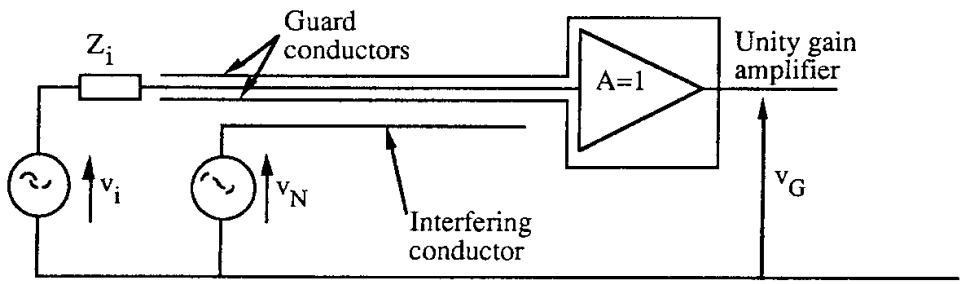
Use of a 'screen'track



Use of a ground plane

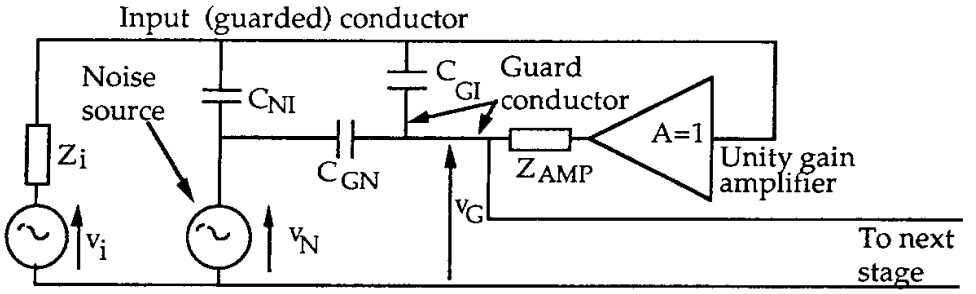
Utilizarea unui traseu ecranat
Utilizarea unui plan legat la masa
Utilizarea unui traseu ecranat si a unui plan legat la pamint pentru protectie

2.2.2. Ecranarea



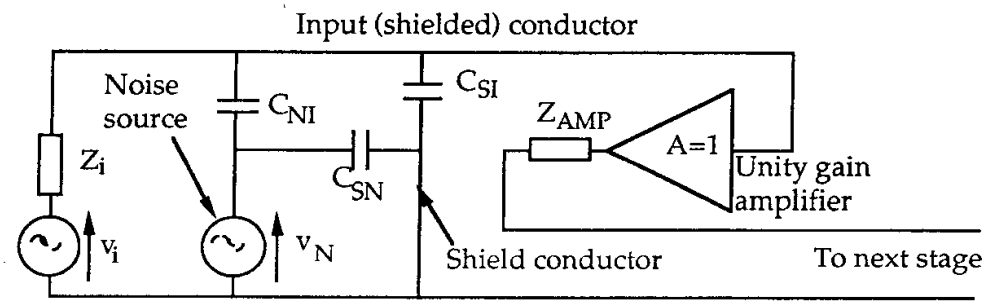
Layout of circuit using guard conductors

Aranjarea elementelor de circuit folosind conductoare de garda



Equivalent circuit with guard conductor in use

Circuitul echivalent cu conductorul de garda in uz

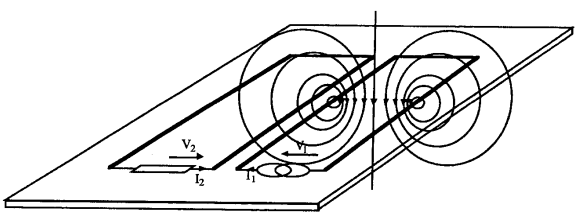


Equivalent circuit with grounded shield conductor instead of guard

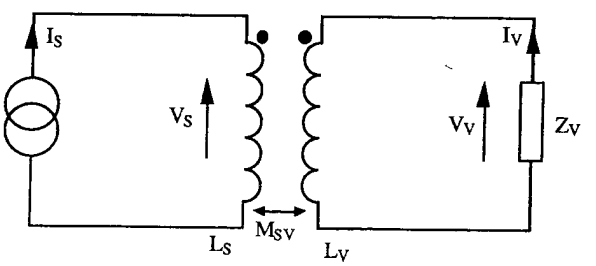
Circuitul echivalent cu conductor ecranat si conectat la masa in loc de ecran
Utilizarea unui conductor de garda pentru reducerea cuplajului capacitiv

2.3. Cuplajul Inductiv

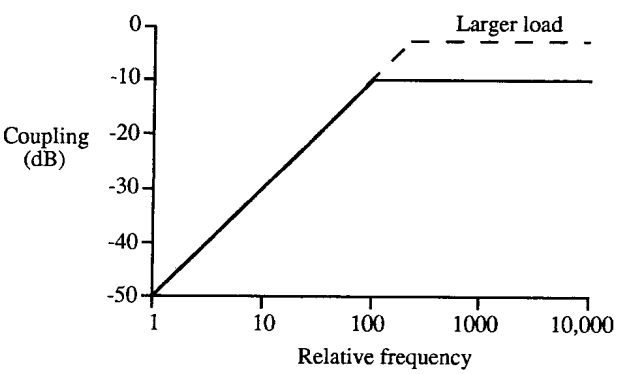
(4) $$E_V = M \frac{dI_S}{dt}$$



Circuite cuplate inductiv

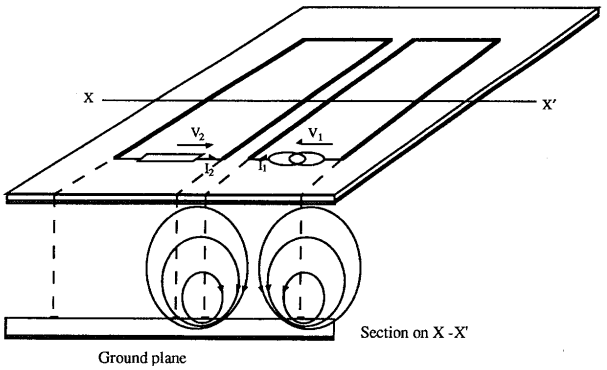


Circuitul echivalent pentru Circuite cuplate inductiv

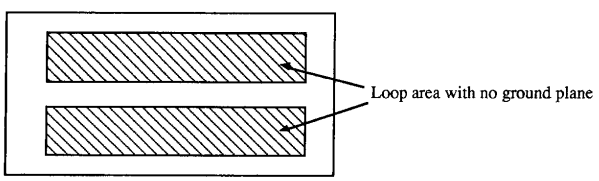


Raspunsul in frecventa a cuplajului dintre bucle adiacente

(5)
$$\frac{V_V}{I_S} = \frac{jw\,M_{VS}}{1 + \frac{jw\,L_V}{Z_V}}$$



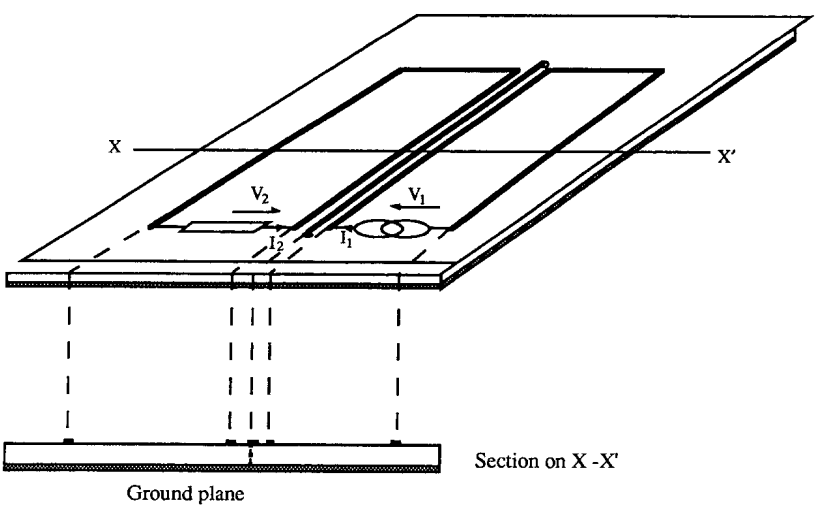
Sectiune prin axa X-X'



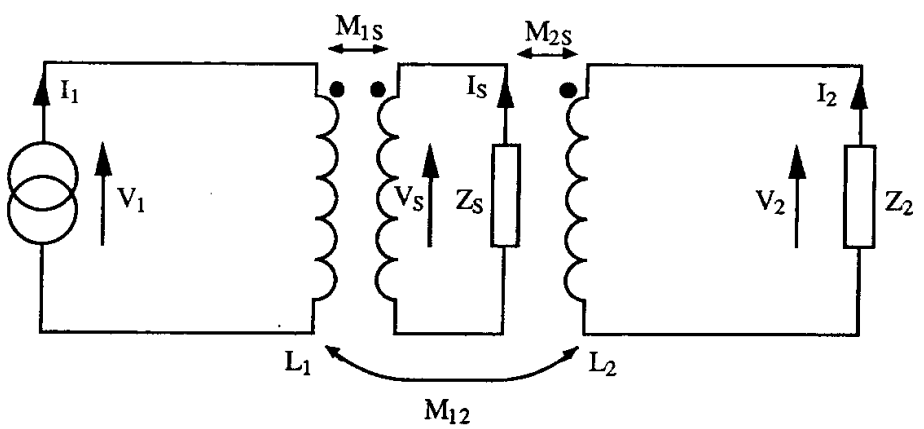
Suprafata buclei fara plan

Suprafata buclei cu plan

O suprafata plana legata la masa reduce suprafata buclei efective pentru frecvente inalte

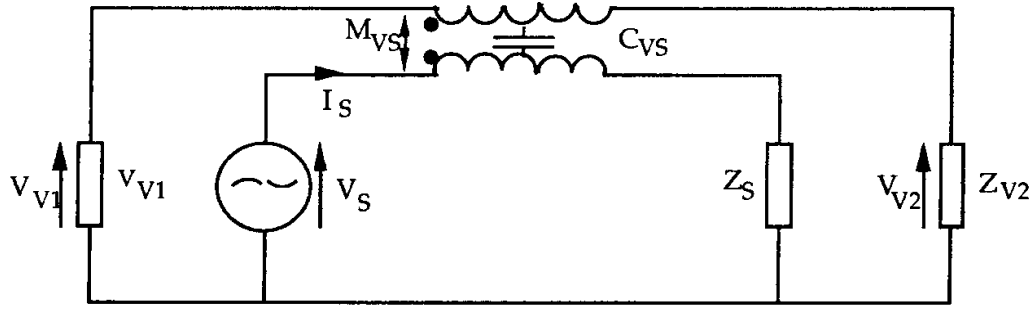


Un traseu ecran conductor dintre circuite cuplate magnetic

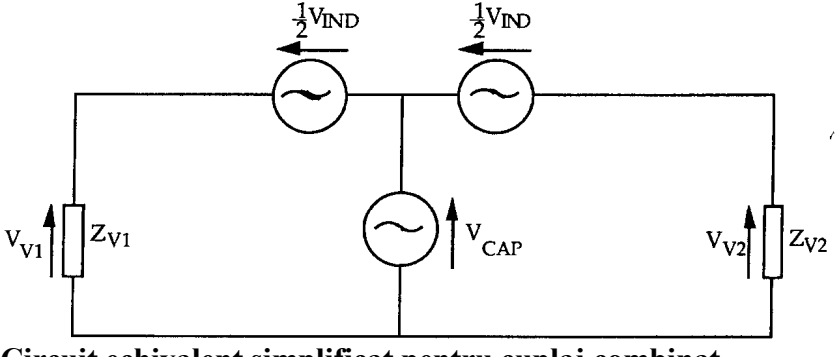


Circuit echivalent a unui ecran conductor dintre circuite cuplate magnetic

2.4. Cuplaj Combinat Capacitiv si Inductiv



Circuit echivalent pentru cuplaj combinat inductiv si capacitiv



Circuit echivalent simplificat pentru cuplaj combinat