

ASYNCHRONOUS COUNTERS

1. Introduction

Counters are sequential logic circuits that counts the pulses applied at their clock input. They usually have 4 bits, delivering at the outputs the corresponding binary code of the number of pulses occurred at the input.

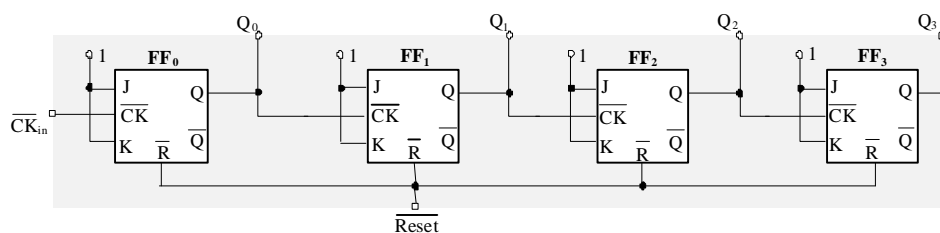
The counters can be classified according to:

- the counting mode:
 - up counters – count up from 0 to the maximum value
 - down counters – count down from the maximum value to 0
 - up/down counters – count up or down under the control of an up or down selection input (reversible).
- the working mode:
 - asynchronous (ripple) counters - the cells are pipelined and they switch successively
 - synchronous counters – the cells switch simultaneously on the same clock.

The basic cell of a counter is the T flip flop. It divides the clock frequency by 2 (when T=logic 1). Connecting n cells, a n bit counter is obtained (2^n maximum capacity). Such counter is in fact a sequential logic circuit with 2^n states. Its output code can be binary (binary counter), BCD (BCD counter), Gray (Gray counter), exponential (exponential counter).

2. Asynchronous binary counter

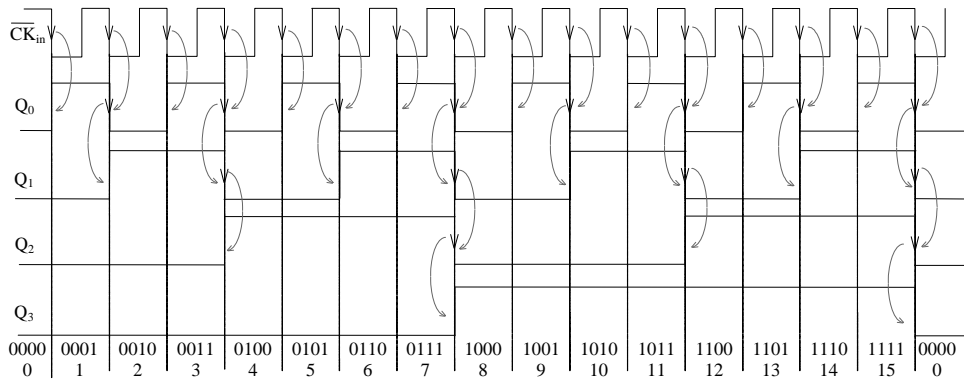
Such a counter has the output of a cell as clock for the next cell $Q_k = \overline{CK_{k+1}}$. In the following figure it represented a 4 bit counter architecture.



The first flip flop (FF₀) has the counter's clock connected at its clock input. It switches (changes the output state) on every clock's falling edge. The second flip flop (FF₁) has as clock the output of FF₀. It switches on

every falling edge on the output Q_0 . The third flip flop (FF_2) has as clock the output of FF_1 . It switches on every falling edge on the output Q_1 . The fourth flip flop (FF_3) has as clock the output of FF_2 . It switches on every falling edge on the output Q_2 . The number of pulses applied at the input can be deduced from the binary code at the outputs:

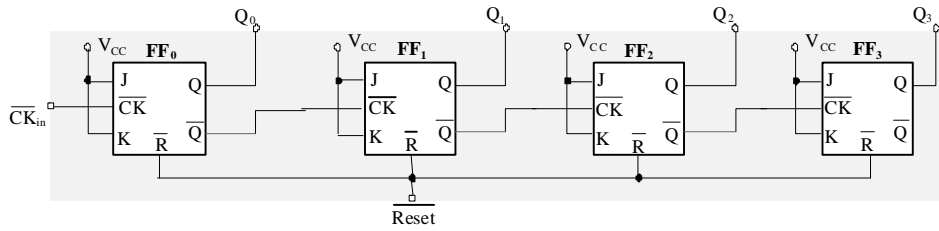
$$N_i = Q_3 \cdot 2^3 + Q_2 \cdot 2^2 + Q_1 \cdot 2^1 + Q_0 \cdot 2^0$$



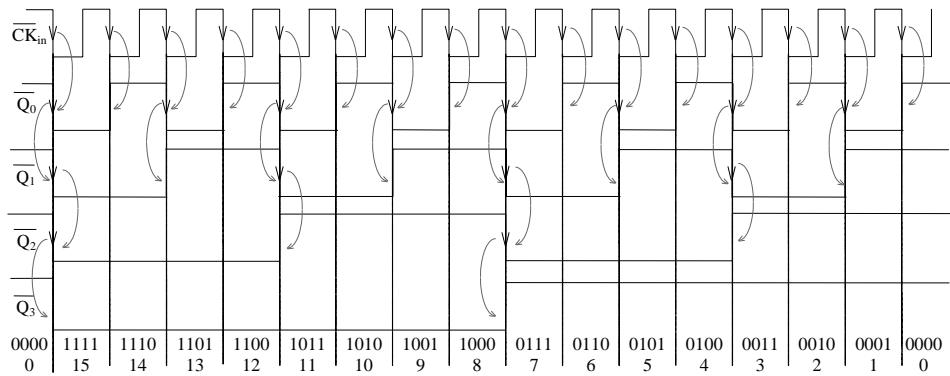
The asynchronous counter can be used in applications where pulses are counted (instruments for measurements). Another application of counters is related to frequency division. Analyzing the waveforms above, the signal on the output Q_0 has the frequency half besides the clock, Q_1 is a quarter besides the clock, Q_2 is one eighth besides the clock and Q_3 is one sixteenth besides the clock. Thus we can say the counters are frequency dividers. The dividing ratios are the powers of 2 (2, 4, 8, 16, etc). If other ratios than 2^n are needed, the counter must count up to the division ratio and then it must be reset. This is achieved with a feedback that detects the final state and reset the counter. Considering the division ratio K , it is transformed in binary $k_3k_2k_1k_0$. The outputs Q_i that correspond to the index i for which $k_i=1$ will be connected through a NAND gate at the Reset input (active on logic 0). After a delay necessary to the signal propagation through circuits, the counter will be initialized (all outputs in logic 0), and the cycle will start again.

3. Down counter

The down counter counts from the maximum value down to zero. If the

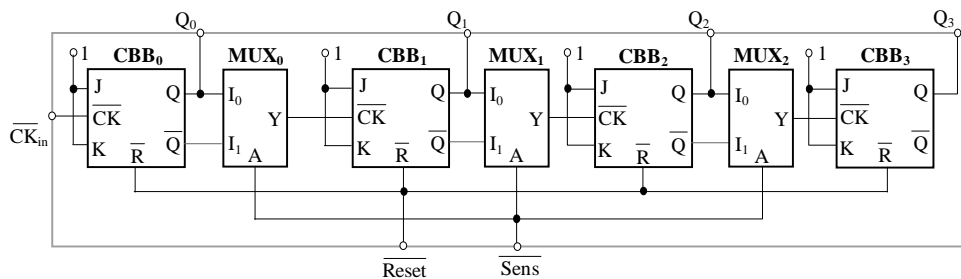


output \overline{Q}_i is connected to the clock input of the next cell, a down asynchronous counter is obtained. The codes at its outputs will follow in the reverse order (from 15 to 0).



4. Reversible asynchronous counter

Analyzing the two counters above, we notice that using a circuit that switches the outputs Q_i or \overline{Q}_i at a cell's clock input, we can change the counting sense. We can use a multiplexer with 2 inputs connected like in the figure below. The address input of all the multiplexers are connected together at the input "Sense". If the input $\overline{Sense}=0 \Rightarrow A=0 \Rightarrow Y=I_0 \Rightarrow$



LAB no. 10.

$\overline{CK}_i = Q_{i-1} \Rightarrow$ the counter counts up. If the input $\overline{Sens} = 1 \Rightarrow A = 1 \Rightarrow Y = I_1$
 $\Rightarrow \overline{CK}_i = \overline{Q_{i-1}} \Rightarrow$ the counter counts down.

3. Lab work

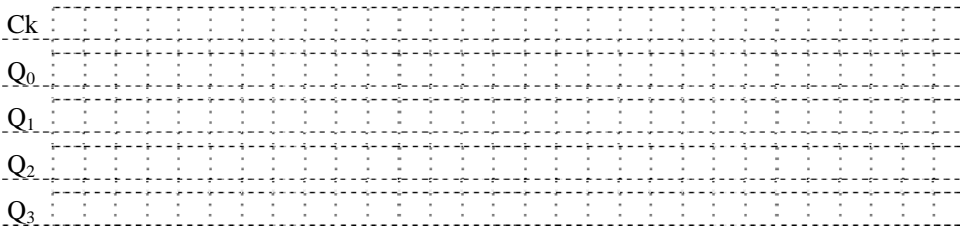
Print the Lab sheet below and complete it according to the indications.

LAB SHEET

1. Input the asynchronous up counter in MaxPlus II and simulate the circuit (16 states, a state is 2 grid periods). Draw the waveforms on the grid below. Measure the delay times (they are different on each output) and write the logic state on the waveforms. Compare the results with the truth table.



2. Input the inverters between the counting cells and simulate the circuit as a new project (16 states, a state is 2 grid periods). Draw the waveforms on the grid below. What kind of counter is this?



3. Input in MaxPlus II the reversible counter and simulate it. Draw the waveforms on the grid below (32 states, a state is 2 grid periods). Write the delay times and the logic states on the waveforms.

