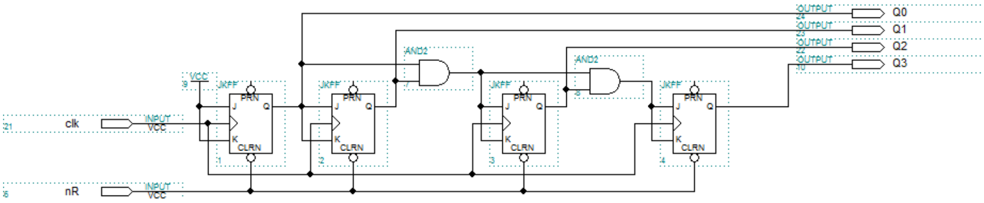
LAB no. 11.

SYNCHROUS COUNTERS

The binary cells of such counter switch simultaneously on the same clock pulse. Its advantages are higher working frequency and no false codes at the outputs.

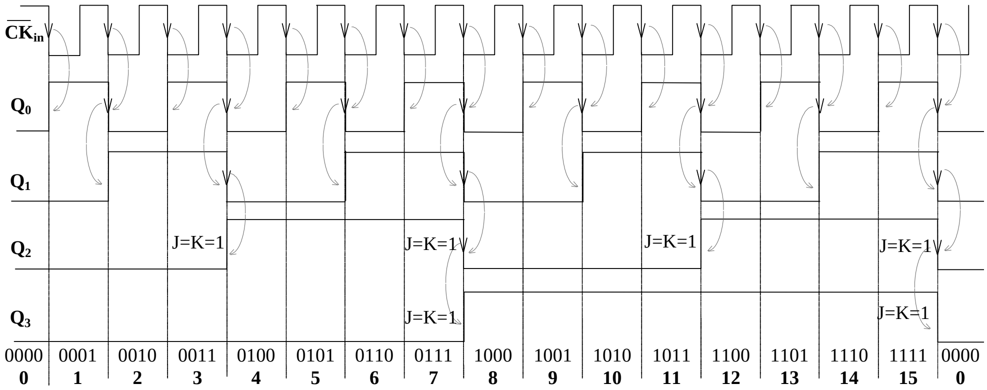
1. Series synchronous binary counter

The logic diagram of this counter is presented in the figure below:



The JK flip-flop switches its logic state when *J*=*K*= logic 1. The AND gates realize the detection of the switching moments. Each cell must switch when all the previous cells are in logic 1. Thus:

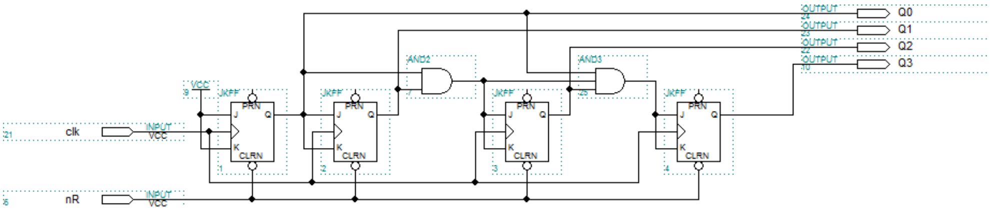
- $JKFF_1$ must switch for each clock pulse applied at its clock input. Its inputs are connected at V_{CC} (logic 1).
- $JKFF_2$ switches every 2 clock pulses, namely only when Q_0 is logic 1. Therefore we will connect $J_1=K_1=Q_0$.
- $JKFF_3$ switches every 4 clock pulses, namely only when Q_0 and Q_1 are logic 1. Therefore we will connect $J_1=K_1=Q_0{\cdot}Q_1$.
- $JKFF_4$ switches every 8 clock pulses, namely only when Q_0 and Q_1 and Q_2 are logic 1. Therefore we will connect $J_1=K_1=Q_0{\cdot}Q_1{\cdot}Q_2$.



The maximum working frequency of a synchronous counter is limited only by the cells switching time and by the AND gates delay time (in the case above 2×t_p).

2. Parallel synchronous binary counter

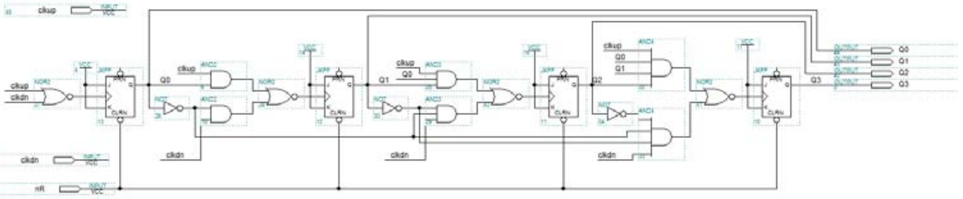
A supplementary increase of speed can be obtained if the AND gates, instead of being cascaded, have the inputs connected directly to the JKFF outputs (next figure).



In this case the maximum working frequency is limited only by the FF switching time and by the delay time of a single gate. It is the fastest counter for a given architecture, but is has the disadvantage that the FF outputs are loaded supplementary with every new stage. Each extra input connected increase the delay time of the FF, reducing the maximum working frequency

3. Reversible synchronous counter

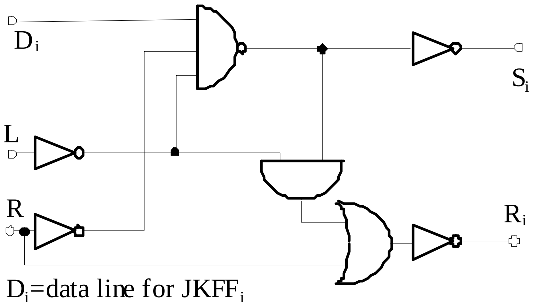
The synchronous counters are built as reversible counters. The logic schematic of such a counter is shown in the following figure:



Each JKFF has its J and K inputs connected to logic 1. The clock is routed to the clock inputs through some kind of multiplexers. The counter has 2 clock signals: if it has clock pulse on the *clkup* input is will count up and if it has clock pulse on the *clkdn* input it counts down. While counting in one sense the other clock input must be in logic 0. The upper AND gates will be opened for clock *clkup* only if Q_0 is logic 1, Q_1 and Q_0 are logic 1 or Q_2 and Q_1 and Q_2 are logic 1. In this case the lower AND gates have the outputs in logic 0 because they are driven by the negated outputs. The counter will count up. The lower gates will be opened for the clok *clkdn* only if Q_0 is logic 0, Q_1 and Q_0 are logic 0 or Q_2 and Q_1 and Q_2 are logic 0. The counter counts down in this case.

- The counter can be transformed into a presetable one using the S and R inputs. The following schematic can be used for each cell in the counter, adding the common input *L* (LOAD) and sepparate data inputs D_0, D_1, D_2, D_3.

Using the parallel load we can realize direct or reverse modulo p counters.



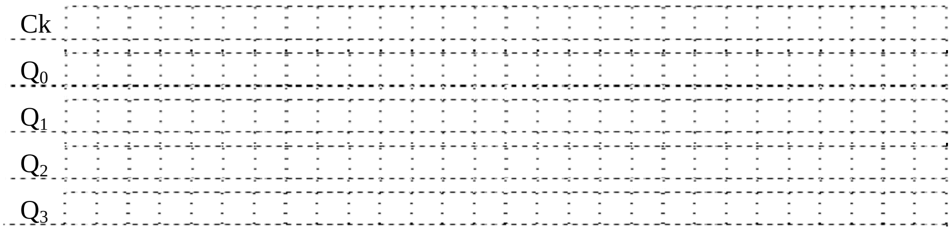
D_i=data line for $JKFF_i$
L=Load
R=Reset

4. Lab works

Complete the following Lab sheet following the indications on it.

LAB SHEET

1. Input the series synchronous binary counter in MaxPlusII and simulate the circuit. Draw the resulted waveforms on the grid below. Write down the delay times and the logic states on the waveforms. Compare the results with the counter's truth table. How are delayed the transitions on the outputs compared with the asynchronous counter?



2. Input the synchronous reversible counter in MaxPlusII. Simulate the circuit for a complete direct counting cycle and a complete reverse counting cycle. Draw the resulted waveforms on the grid below and write down the delays on the outputs and the logic states.

3. Synthesize a synchronous BCD counter using the VX diagrams method.

	t_n				t_{n+1}											
N_z	Q_3	Q_2	Q_1	Q_0	Q_3	Q_2	Q_1	Q_0	J_3	K_3	J_2	K_2	J_1	K_1	J_0	K_0
0	0	0	0	0												
1	0	0	0	1												
2	0	0	1	0												
3	0	0	1	1												
4	0	1	0	0												
5	0	1	0	1												
6	0	1	1	0												
7	0	1	1	1												
8	1	0	0	0												
9	1	0	0	1												

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VK diagrams:

	J_3				K_3				J_2				K_2			
Q_3Q_2 \ Q_1Q_0	00	01	11	10	00	01	11	10	00	01	11	10	00	01	11	10
00																
01																
11																
10																
00																
01																
11																
10																
	J_1				K_1				J_0				K_0			

J_0= K_0=

J_1= K_1=

J_2= K_2=

J_3= K_3=

4. Input the schematic above in MaxPlus II and simulate it. Draw the waveforms on the grid below and write down the logic states on the waveforms and the delays between the outputs.