DECODERS I

Decoders are combinational logic circuits that activate one or more outputs, according to code applied at its inputs. Their applications are memory addressing digital display, data multiplexing, etc.

1. Address decoder with enable inputs

This type of decoder is used for memory addressing in microprocessor systems. The circuit activates a single output corresponding to the input code. The activation occures only if the enable inputs are activated (the circuit is selected).

Such a very used circuit is 74LS138 (fig.1), whosw truth table is shown below:

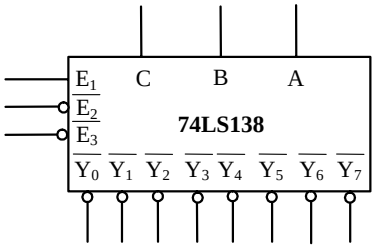


Figure 1

E_1	$\overline{E_2}$	$\overline{E_3}$	C	B	A	$\overline{Y_7}$	$\overline{Y_6}$	$\overline{Y_5}$	$\overline{Y_4}$	$\overline{Y_3}$	$\overline{Y_2}$	$\overline{Y_1}$	$\overline{Y_0}$	**Remarks**
0	X	X	X	X	X	1	1	1	1	1	1	1	1	circuit is off
X	1	X	X	X	X	1	1	1	1	1	1	1	1	circuit is off
X	X	1	X	X	X	1	1	1	1	1	1	1	1	circuit is off
1	0	0	0	0	0	1	1	1	1	1	1	1	0	Y_0 is active
1	0	0	0	0	1	1	1	1	1	1	1	0	1	Y_1 is active
1	0	0	0	1	0	1	1	1	1	1	0	1	1	Y_2 is active
1	0	0	0	1	1	1	1	1	1	0	1	1	1	Y_3 is active
1	0	0	1	0	0	1	1	1	0	1	1	1	1	Y_4 is active
1	0	0	1	0	1	1	1	0	1	1	1	1	1	Y_5 is active
1	0	0	1	1	0	1	0	1	1	1	1	1	1	Y_6 is active
1	0	0	1	1	1	0	1	1	1	1	1	1	1	Y_7 is active

The circuit has 3 inputs (A, B, C) for the code word (address):

$$\overline{Y_i} = 0 \Leftarrow i\big|_Z = CBA\big|_B = C \cdot 2^2 + B \cdot 2^1 + A \cdot 2^0\big|_Z$$

and 3 inputs for circuit selection (circuit enable): one active on logic 1 (E_1) and 2 active on logic 0 ($\overline{E_2}$ and $\overline{E_3}$). The circuit is selected (active) when all three enable inputs are active (E_1 is active AND $\overline{E_2}$ is active AND $\overline{E_3}$ is active). Those three variables can be replaced with a single one $E = E_1 \cdot \overline{E_2} \cdot \overline{E_2}$ for simplifying the synthesis. The truth table can be rewritten for 4 input variables.

2. BCD to decimal decoder

In practice we frequently find situations when we need to decode a BCD (Binary to decimal) code – for example displaying on Nixie tubes. This is similar with the address decoder, except it has ten outputs. The truth table is shown below.

D	C	B	A	$\overline{Y_9}$	$\overline{Y_8}$	$\overline{Y_7}$	$\overline{Y_6}$	$\overline{Y_5}$	$\overline{Y_4}$	$\overline{Y_3}$	$\overline{Y_2}$	$\overline{Y_1}$	$\overline{Y_0}$	**Remarks**
0	**0**	**0**	**0**	1	1	1	1	1	1	1	1	1	0	Y_0 is active
0	**0**	**0**	**1**	1	1	1	1	1	1	1	1	0	1	Y_1 is active
0	**0**	**1**	**0**	1	1	1	1	1	1	1	0	1	1	Y_2 is active
0	**0**	**1**	**1**	1	1	1	1	1	1	0	1	1	1	Y_3 is active
0	**1**	**0**	**0**	1	1	1	1	1	0	1	1	1	1	Y_4 is active
0	**1**	**0**	**1**	1	1	1	1	0	1	1	1	1	1	Y_5 is active
0	**1**	**1**	**0**	1	1	1	0	1	1	1	1	1	1	Y_6 is active
0	**1**	**1**	**1**	1	1	0	1	1	1	1	1	1	1	Y_7 is active
1	**0**	**0**	**0**	1	0	1	1	1	1	1	1	1	1	Y_8 is active
1	**0**	**0**	**1**	0	1	1	1	1	1	1	1	1	1	Y_9 is active
1	**0**	**1**	**0**	1	1	1	1	1	1	1	1	1	1	outputs off
1	**0**	**1**	**1**	1	1	1	1	1	1	1	1	1	1	outputs off
1	**1**	**0**	**0**	1	1	1	1	1	1	1	1	1	1	outputs off
1	**1**	**0**	**1**	1	1	1	1	1	1	1	1	1	1	outputs off
1	**1**	**1**	**0**	1	1	1	1	1	1	1	1	1	1	outputs off
1	**1**	**1**	**1**	1	1	1	1	1	1	1	1	1	1	outputs off

The circuit works only with BCD input code. We can consider the outputs for the input combinations greater than 9 (1001) as being don't care in order to obtain a simpler circuit. The above table is complete and no output will be active for the codes greater than 9. The circuit will be more complicated in this case.

3. Works to do in the lab

Complete the following sheet according to the indications.

LAB SHEET

1. Starting from the reduced truth table complete the VK diagrams below and extract the minimized equations for the 8 outputs.

BA \ EC	00	01	11	10
00				
01				
11				
10				

$\overline{Y_0}$ =

BA \ EC	00	01	11	10
00				
01				
11				
10				

$\overline{Y_1}$ =

BA \ EC	00	01	11	10
00				
01				
11				
10				

$\overline{Y_2}$ =

BA \ EC	00	01	11	10
00				
01				
11				
10				

$\overline{Y_3}$ =

BA \ EC	00	01	11	10
00				
01				
11				
10				

$\overline{Y_4}$ =

BA \ EC	00	01	11	10
00				
01				
11				
10				

$\overline{Y_5}$ =

BA \ EC	00	01	11	10
00				
01				
11				
10				

$\overline{Y_6}$ =

BA \ EC	00	01	11	10
00				
01				
11				
10				

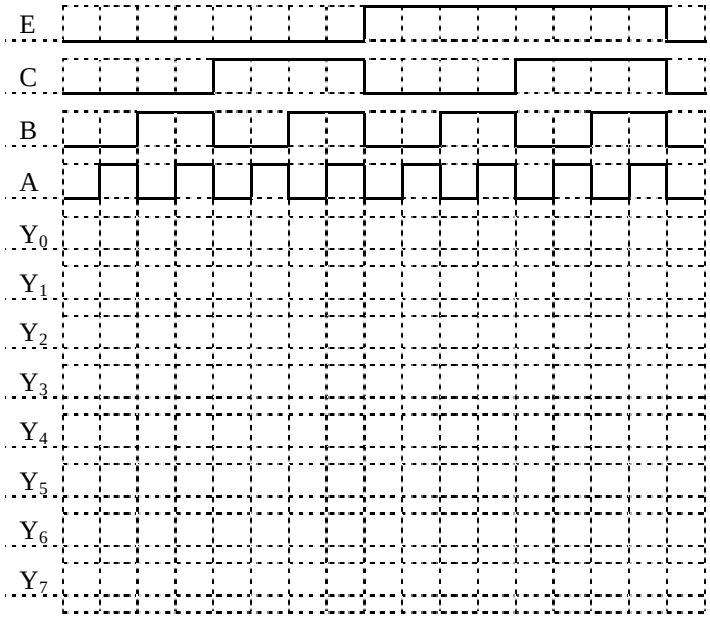
$\overline{Y_7}$ =

LAB no. 4.

2. From the equations deduced at 1st requirement, build the circuit of the address decoder with logic gates:

3. Introduce the circuit in MaxPlusII and simulate it. Draw the waveforms resulted from simulation below. Determine the delay time between in and out.

Waveforms:



t_d=