## DECODERS II

## 1. BCD to 7 segments decoder

BCD to 7 segments decoders are logic circuits designed for driving 7 segments display cells (LEDs, bulbs, LCD or gas discharge tubes).

The circuit has 4 inputs, usually named A, B, C, D and 7 outputs a, b, c, d, e, f, g. The inputs codify a 4 bits binary number with $A=L S B^{1)}$ and $\mathrm{D}=\mathrm{MSB}^{2)}$. The display device is presented in figure 1 and it is usually called digit. In practice there are displays with LEDs (Light Emitting Diodes) connected with common anodes (AC) or with common cathode (CK). In the first case the display is driven with low logic voltage ( L or 0 ) and in the second case it is driven with high logic voltage (H or 1 ).


Segments arrangement allows the display of numbers from 0 to 9 (figure 2 a and b ) and even of some letters (figure 2.c for display in hexadecimal).

[^0]a）


b）


c）



Figure 2
Most display circuits use the numbers in figure 2．a or rarely those in figure 2．b． The truth table of such circuit is presented below：

The truth table of the BCD to 7 segments decoder

| $\mathrm{N}_{\mathbf{z}}$ | D | C | B | A | a | b | c | d | e | f | g |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | 0 | 0 | 0 | 0 |  |  |  |  |  |  | 区 |
| 1 | 0 | 0 | 0 | 1 | 区 |  |  | 区 | 区 | 区 | 区 |
| 2 | 0 | 0 | 1 | 0 |  |  | 区 |  |  | 区 |  |
| 3 | 0 | 0 | 1 | 1 |  |  |  |  | 区 | 区 |  |
| 4 | 0 | 1 | 0 | 0 | 区 |  |  | 区 | 区 |  |  |
| 5 | 0 | 1 | 0 | 1 |  | 区 |  |  | 区 |  |  |
| 6 | 0 | 1 | 1 | 0 |  | 区 |  |  |  |  |  |
| 7 | 0 | 1 | 1 | 1 |  |  |  | 区 | 区 | 区 | 区 |
| 8 | 1 | 0 | 0 | 0 |  |  |  |  |  |  |  |
| 9 | 1 | 0 | 0 | 1 |  |  |  |  | 区 |  |  |

At the 4 inputs a BCD code is applied that represents the code of number to be displayed．The 7 outputs are connected to the corresponding segments of the display cell through resistors in order to limit the current．

Starting from the truth table we can build the 7 VK diagrams for synthesize the circuit．Depending on the cell type，segment on can be logic 0 for AC or logic 1 for CK．

## LAB no. 5.

## 2. Implementing logic functions with decoders

Using decoders for implementing logic functions has the advantage that no minimization is necessary. Implementations with reduced costs can be obtained in some cases (just 1 integrated circuit). We start from the disjunctive canonical form because the decoder outputs implement the negated miniterms. The implementation means connecting the outputs corresponding to th miniterms in the function through a NAND gate or connecting the missing miniterms through an AND gate. The first solution is frequently used because we can find NAND gates with 8 inputs as integrated circuits.

Let us consider the following function:

$$
f(a, b, c)=a \cdot \bar{b}+\bar{a} \cdot b \cdot c+a \cdot c+b \cdot c
$$

The equation can be rewritten as:

$$
f(a, b, c)=\overline{\left(\overline{m_{1}+m_{5}+m_{6}+m_{7}}\right)}=\overline{\overline{m_{1}}+\overline{m_{5}}+\overline{m_{6}}+\overline{m_{7}}}
$$

Using the BCD to decimal decoder (SN 442) the circuits in figure 3 show the implementation of the above function.


Figura 3

## 3. Works to do in the lab

Complete the following sheet according to the indications.

## LAB SHET

1. Complete the following truth table using the figure 2.b for common anode display.

| Nr. | D | C | B | A | a | b | c | d | e | f | g |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 |  |  |  |  |  |  |  |  |  |  |  |

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| 1 |  |  |  |  |  |  |  |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- | :--- |
| 2 |  |  |  |  |  |  |  |  |  |  |  |
| 3 |  |  |  |  |  |  |  |  |  |  |  |
| 4 |  |  |  |  |  |  |  |  |  |  |  |
| 5 |  |  |  |  |  |  |  |  |  |  |  |
| 6 |  |  |  |  |  |  |  |  |  |  |  |
| 7 |  |  |  |  |  |  |  |  |  |  |  |
| 8 |  |  |  |  |  |  |  |  |  |  |  |
| 9 |  |  |  |  |  |  |  |  |  |  |  |

2. Fill in the VK diagrams and determine the minimized functions:

| DC <br> BA | 00 | 01 | 11 | 10 |
| :--- | :--- | :--- | :--- | :--- |
| 00 |  |  |  |  |
| 01 |  |  |  |  |
| 11 |  |  |  |  |
| 10 |  |  |  |  |


| DC <br> BA | 00 | 01 | 11 | 10 |
| :--- | :--- | :--- | :--- | :--- |
| 00 |  |  |  |  |
| 01 |  |  |  |  |
| 11 |  |  |  |  |
| 10 |  |  |  |  |


| c $=$ |
| :--- |
| DC <br> BA 00 01 11 10 <br> 00     <br> 01     <br> 11     <br> 10     |
| $\mathrm{e}=$ |


| DC <br> BA | 00 | 01 | 11 | 10 |
| :--- | :--- | :--- | :--- | :--- |
| 00 |  |  |  |  |
| 01 |  |  |  |  |
| 11 |  |  |  |  |
| 10 |  |  |  |  |


| $\mathrm{b}=$ |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- |
| DC <br> BA | 00 | 01 | 11 | 10 |
| 00 |  |  |  |  |
| 01 |  |  |  |  |
| 11 |  |  |  |  |
| 10 |  |  |  |  |
| $\mathrm{~d}=$ |  |  |  |  |


| DC <br> BA | 00 | 01 | 11 | 10 |
| :--- | :--- | :--- | :--- | :--- |
| 00 |  |  |  |  |
| 01 |  |  |  |  |
| 11 |  |  |  |  |
| 10 |  |  |  |  |
| $\mathrm{f}=$ |  |  |  |  |


| DC <br> BA | 00 | 01 | 11 | 10 |
| :--- | :--- | :--- | :--- | :--- |
| 00 |  |  |  |  |
| 01 |  |  |  |  |
| 11 |  |  |  |  |

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| 10 |  |  |  |  |
| :--- | :--- | :--- | :--- | :--- |
| $\mathrm{~g}=$ |  |  |  |  |

3. Draw the minimized circuit schematic with logic gates starting from the equations found above.
4. Input the schematic in MaxPlusII and simulate the circuit. Draw the waveforms obtained in the simulation below. Find out the delay times and mark the logic states (0 or1) on to the waveforms. Compare the results with the truth table.


5. What are the symbols displayed for the input codes from 10 to 15 ?

[^0]:    ${ }^{1)}$ LSB $=$ Least Significant Bit
    ${ }^{2)}$ MSB $=$ Most Significant Bit

