MULTIPLEXERS

Multiplexers are combinational logic circuits that switch the data from oneof its input to a unique output. The input is selected through an address word.

1. 2 to 1 multiplexer

The circuit allows switching the data from the input I_0 (A=0) or I_1 (A=1) toward the output Y. The circuit symbol and its truth table are presented in figure 1.
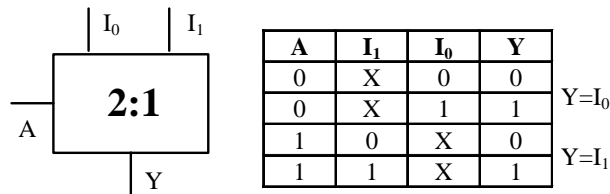
A	I_1	I_0	Y	
0	X	0	0	
0	X	1	1	$Y=I_0$
1	0	X	0	
1	1	X	1	$Y=I_1$

Figure 1

The correspondingVK diagram is shown below. By grouping the cells that contain logic 1 we get the equation:

I_1I_0 / A	00	01	11	10
0	0	0	1	1
1	0	1	1	0

$$Y = \overline{A} \cdot I_0 + A \cdot I_1 \ .$$

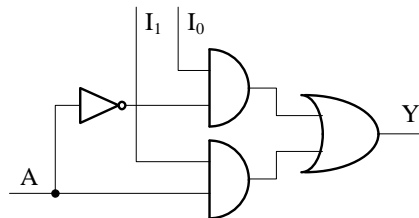From this equation, the multiplexer will look like in figure 2:

Figure 2

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2. 4:1 multiplexer with enable input

For addressing 4 inputs, 2 address lines are necessary. Their selection is similar with the one in the address decoder. The circuit has an additional input for enabling its operation.

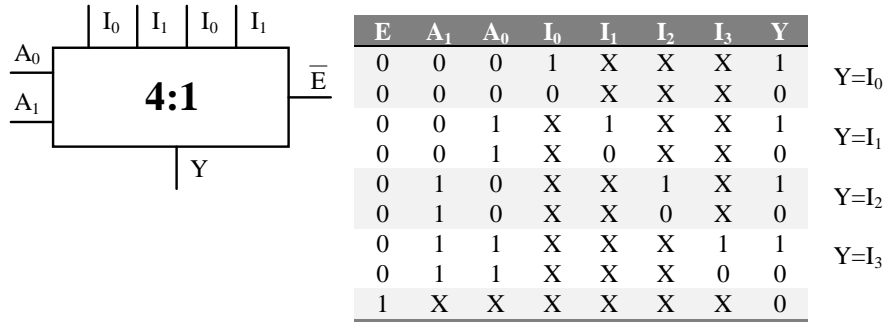The circuit symbol and its truth table are presented in figure 3.

E	A_1	A_0	I_0	I_1	I_2	I_3	Y	
0	0	0	1	X	X	X	1	$Y=I_0$
0	0	0	0	X	X	X	0	
0	0	1	X	1	X	X	1	$Y=I_1$
0	0	1	X	0	X	X	0	
0	1	0	X	X	1	X	1	$Y=I_2$
0	1	0	X	X	0	X	0	
0	1	1	X	X	X	1	1	$Y=I_3$
0	1	1	X	X	X	0	0	
1	X	X	X	X	X	X	0	

Figura 3

The VK diagram associated with this circuit is the following:

$I_3I_2I_1I_0$ / EA_1A_0	0000	0001	0011	0010	0110	0111	0101	0100	1100	1101	1111	1110	1010	1011	1001	1000
0 0 0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
0 0 1	0	0	1	1	1	1	0	0	0	0	1	1	1	1	0	0
0 1 1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
0 1 0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0
1 1 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1 1 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1 0 1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1 0 0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

$$Y = \overline{E} \cdot \overline{A_1} \cdot \overline{A_0} \cdot I_0 \cdot (\overline{I_2} \cdot \overline{I_3} + \overline{I_3} \cdot I_2 + I_3 \cdot I_2 + I_3 \cdot \overline{I_2}) +$$
$$+ \overline{E} \cdot \overline{A_1} \cdot A_0 \cdot I_1 \cdot (\overline{I_3} + I_3) + \overline{E} \cdot A_1 \cdot \overline{A_0} \cdot I_2 + \overline{E} \cdot A_1 \cdot A_0 \cdot I_3 =$$
$$= \overline{E} \cdot (\overline{A_1} \cdot \overline{A_0} \cdot I_0 + \overline{A_1} \cdot A_0 \cdot I_1 + A_1 \cdot \overline{A_0} \cdot I_2 + A_1 \cdot A_0 \cdot I_3)$$

The synthesis needs : - 1 OR gate with 4 inputs
- 4 AND gates with 4 inputs
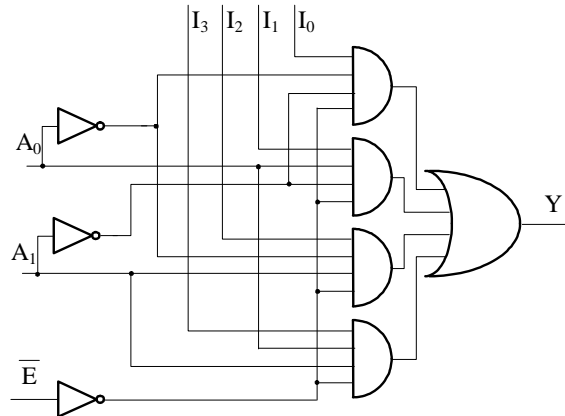- 3 inverters

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Figure 4

3. Implementation of logic functions using multiplexers

Any logic function can be written as a sum of miniterms:

$$f = \sum_{i=0}^{2^n-1} m_i \cdot k_i \tag{1}$$

where: - $k_i=0$ if the miniterm does not appear in the disjunction

        - $k_i=1$ if the miniterm appears in the disjunction

The generalized equation of a multiplexer is:

$$Y = \overline{E} \cdot \sum_{i=0}^{2^n-1} m_i \cdot I_i \tag{2}$$

Comparing the equations (1) and (2) we can conclude that any logic function can be implemented using a multiplexer by connecting the input $\overline{E}$ to logic 0 and the inputs I_i to logic 1 respectively to logic 0 if the miniterm appears in function or not.

Example:

Considerring the function $\qquad f = \overline{A} \cdot B \cdot C + A \cdot \overline{B} \cdot C + A \cdot B \cdot \overline{C}$

it can be rewritten:

$$f = \underbrace{\overline{A} \cdot \overline{B} \cdot \overline{C}}_{I_0} \cdot 0 + \underbrace{A \cdot \overline{B} \cdot \overline{C}}_{I_1} \cdot 0 + \underbrace{\overline{A} \cdot B \cdot \overline{C}}_{I_2} \cdot 0 + \underbrace{A \cdot B \cdot \overline{C}}_{I_3} +$$

$$+ \underbrace{\overline{A} \cdot \overline{B} \cdot C}_{I_4} \cdot 0 + \underbrace{A \cdot \overline{B} \cdot C}_{I_5} + \underbrace{\overline{A} \cdot B \cdot C}_{I_6} + \underbrace{A \cdot B \cdot C}_{I_7} \cdot 0$$

33

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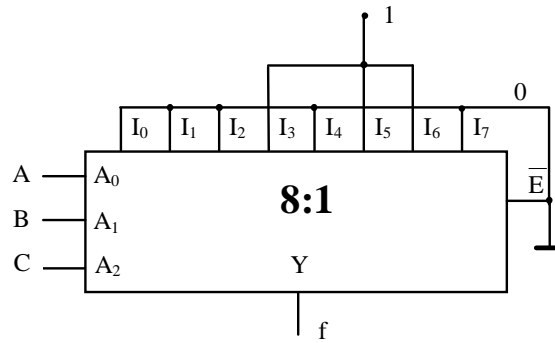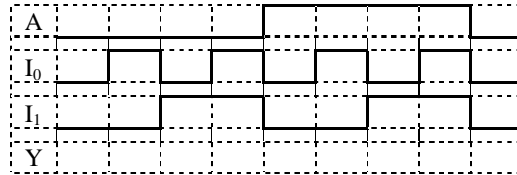
The function implementation can be done like below:

Figure 5

4. Lab works

Complete the following sheet according to the indications.

LAB no. 6.

LAB SHEET

1. Make the 2 :1 multiplexer schematic in MaxPlus II (figure 2). Simulate it and draw the output waveform on the grid below. Compare the resulted data with the truth table.

2. Make the 4:1 multiplexer in MaxPlusII (figure 4). Simulate and draw the output waveform $\overline{E} = 0$. Find the delay time and mark the logic values on the waveforms. Compare the results with the truth table.