LAB no. 7

COMPARATOARE NUMERICE

Digital comparators are combinational logic circuits that detect the relative value of 2 binary numbers. Such circuit has a symbol like in figure 1 and has $2\times n$ inputs for the 2 numbers and 3 outputs: $A>B$, $A=B$ şi $A<B$.

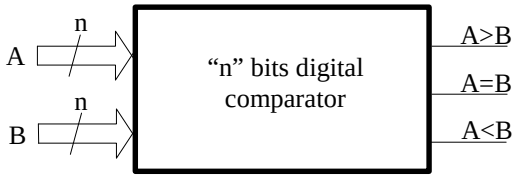

Figure 1

1. 1 bit digital comparator

This circuit allows comparing 2 numbers of 1 bit each, indicating on the 3 outputs the relation between them: >, =, <. This is a particular case of the above

A_i	B_i	y_1	y_2	y_3
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

Figure 2

case, with $n=1$. The symbol and the truth table of the circuit are presented in figure 2.

The output y_i is logic 1 when the input numbers respect the relation corresponding to the output, in the rest being logic 0. The associated VK diagrams are the following:

A_i \ B_i	0	1
0	0	(1)
1	0	0

$y_1=\overline{A_i}\cdot B_i$

A_i \ B_i	0	1
0	(1)	0
1	0	(1)

$y_2=\overline{A_i}\cdot\overline{B_i}+ A_i\cdot B_i= \overline{A_i\oplus B_i}$

A_i \ B_i	0	1
0	0	0
1	(1)	0

$y_3=A_i\cdot\overline{B_i}$

From the equations deduced above we can build the circuit from figure 3.

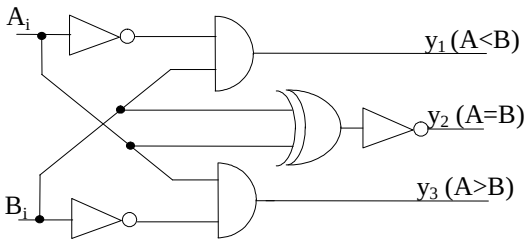

Figure 3

2. 2 bits digital comparator

Using two 1 bit comparators we can build a 2 bits comparator. The numbers to be compared have the decimal equivalents:

$$A = A_0 \cdot 2^0 + A_1 \cdot 2^1$$

$$B = B_0 \cdot 2^0 + B_1 \cdot 2^1$$

Comparing binary numbers give the same results as comparing their decimal equivalents. The comparison follows the logic diagram shown in figure 4.

The comparison starts with the most significant A_1 and B_1. If $A_1>B_1$ or $A_1<B_1$ we can deduce that $A>B$ and respectively $A<B$, no matter what are the bits A_0 and B_0.

If $A_1=B_1$, for establishing the relation between the 2 numbers, we have to look for the relation between A_0 and B_0. If $A_0=B_0$ the output Y_2 ($A=B$) will be activated. If $A_0>B_0$ or $A_0<B_0$ then $A>B$ or respectively $A<B$ and the corresponding output will be activated.

This reasoning can be extended for many bits. Another alternative assume to build the truth table and using the VK diagrams to minimize the logic functions and make the schematic with logic gates. This will be used in the following.

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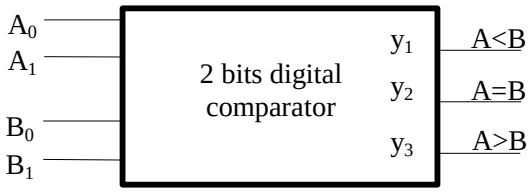

Figure 4

3. Lab work

Print the Lab sheet below and complete it according to the indications.

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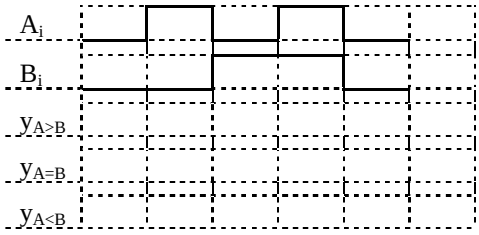
LAB SHEET

1. Introduce the schematic from figure 3 in MaxPlus II and simulate the circuit. Draw the waveforms obtained from simulation respecting the delays. Write the delay times and the logic valeu on the waveforms. Compare the results with the truth table.



2. Complete the the 2 bits digital comparator truth table.

B_1	B_0	A_1	A_0	$y_{A>B}$	$y_{A=B}$	$y_{A<B}$
0	0	0	0			
0	0	0	1			
0	0	1	0			
0	0	1	1			
0	1	0	0			
0	1	0	1			
0	1	1	0			
0	1	1	1			
1	0	0	0			
1	0	0	1			
1	0	1	0			
1	0	1	1			
1	1	0	0			
1	1	0	1			
1	1	1	0			
1	1	1	1			

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3. Synthesize the 2 bits comparator using the VK diagrams.

B_1B_0 / A_1A_0	00	01	11	10
00				
01				
11				
10				

$y_{A>B}$ =

B_1B_0 / A_1A_0	00	01	11	10
00				
01				
11				
10				

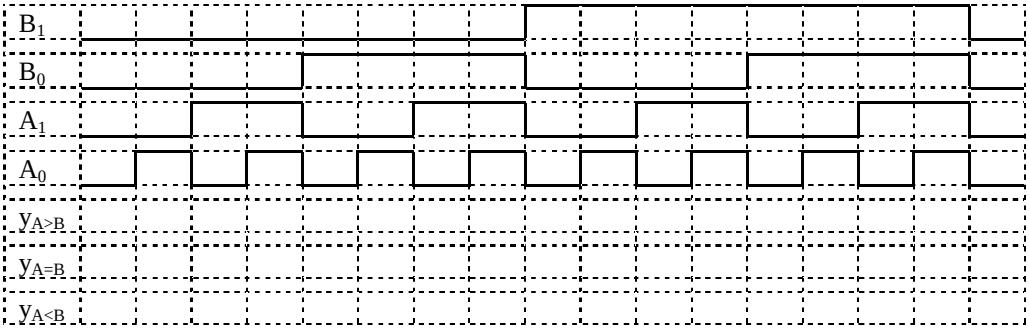
$y_{A=B}$ =

B_1B_0 / A_1A_0	00	01	11	10
00				
01				
11				
10				

$y_{A<B}$ =

4. Implement the 2 bits comparator with logic gates and draw it below.

5. Simulate the 2 bits comparator in MaxPlusII and draw the waveforms respecting the delays. Write the delay and the logic states on the waveforms.



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