

## DIGITAL ADDERS

In digital systems, especially in the internal structure of a microprocessor, math operations are necessary. The fundamental operation, on which basis are executed the other operations, is the addition. The subtraction is executed by adding the minuend with the subtrahend's complement. The multiplication and the division mean multiple additions or subtractions. The block that realizes the addition is called adder.

Considering 2 binary numbers:

$$X = x_{n-1}x_{n-2}\dots x_2x_1x_0 \big|_2$$

$$Y = y_{n-1}y_{n-2}\dots y_2y_1y_0 \big|_2$$

where  $x_i$  and  $y_i$  are binary numbers (0 or 1). The sum,  $X+Y$ , has the following structure:

$$S = X + Y = t_n s_{n-1} s_{n-2} \dots s_2 s_1 s_0 \big|_2$$

Adding the numbers is similar with the addition in the decimal base, but bit by bit in the computation base 2:

$$\begin{array}{r}
 x_{n-1}x_{n-2}\dots x_2x_1x_0 + \\
 y_{n-1}y_{n-2}\dots y_2y_1y_0 \\
 \hline
 t_n s_{n-1} s_{n-2} \dots s_2 s_1 s_0 \\
 \underbrace{\phantom{t_n s_{n-1} s_{n-2} \dots s_2 s_1 s_0}}_{\substack{\curvearrowright \quad \curvearrowright \quad \curvearrowright \quad \curvearrowright \quad \curvearrowright \quad \curvearrowright \\ t_{n-1} \quad t_{n-2} \quad t_{n-3} \quad t_2 \quad t_1 \quad t_0}}
 \end{array}$$

### 1. Elementary half-adder

This circuit realizes the addition of 2 singular bits. It can be used for adding the bits on the least significant range (range 0) of two binary numbers. The circuit has 2 inputs, one for each bit, and 2 outputs: one for the sum and the other for transport (carry bit). Because we have only two possibilities for each bit, there are four cases:  $0+0=0$ ,  $0+1=1$ ,  $1+0=1$  and  $1+1=10|_2$ . In the last case, 0 is the sum (s) and 1 is the carry bit (t). The circuit truth table is:

x	y	s	t
0	0	0	0

0	1	1	0
1	0	1	0
1	1	0	1

where  $s$  is the sum (the range  $2^0$  bit), and  $t$  is the carry bit for the next range (the range  $2^1$  bit). The VK diagrams for this circuit are

$x \backslash y$	0	1
0	0	1
1	1	0

$x \backslash y$	0	1
0	0	0
1	0	1

$$s = y \cdot \bar{x} + x \cdot \bar{y} = x \oplus y$$

$$t = x \cdot y$$

According to the above equations, the circuit can be implemented with two logic gates like in figure 1:

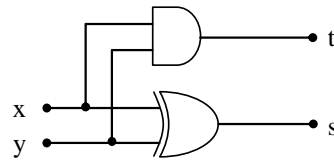
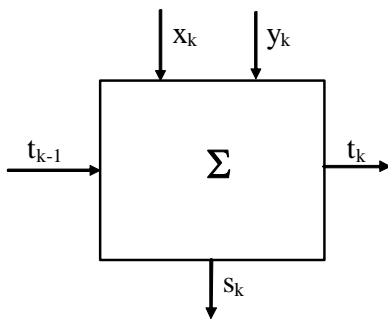


Figure 1

## 2. Elementary full adder

The addition of two binary numbers has as result a number with the same number of bits as the operands and one more carry bit toward to the next range. For the addition of any two bits in a sum we use an elementary full adder. The circuit symbol and the truth table of the full adder are presented in figure 2.



$y_k$	$x_k$	$t_{k-1}$	$s_k$	$s_{k+1}=t_k$
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Figure 2

From the truth table above we complete the VK diagrams.

$y_k x_k \backslash t_{k-1}$	00	01	11	10
0	0	1	0	1
1	1	0	1	0

$$s_k = x_k \oplus y_k \oplus t_{k-1}$$

$y_k x_k \backslash t_{k-1}$	00	01	11	10
0	0	0	1	0
1	0	1	1	1

$$t_k = x_k \cdot y_k + t_{k-1} \cdot (x_k \cdot y_k + x_k \cdot y_k)$$

The resulted logic equations lead to the following schematic:

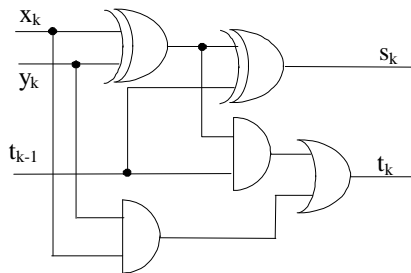


Figure 3

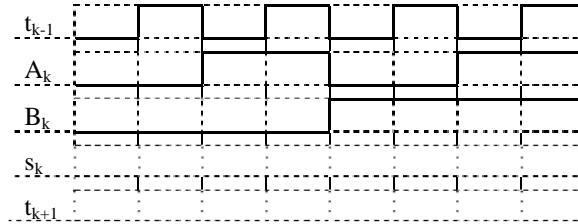
Full adders can be cascaded in order to create a  $n$  bit adder (ripple carry adder). The carry bit from one stage goes to the next stage, thus, the last stage must wait for the carry to propagate along all the other adders.

### 3. Lab work

Print the Lab sheet below and complete it according to the indications.

**LAB SHEET**

1. Introduce the schematic in figure 3 in MaxPlusII and simulate it. Draw the waveforms resulted from simulation on the grid below. Write down the delay times and the logic values on the waveforms. Compare the results with the truth table.

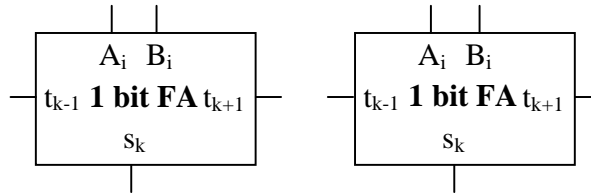


2. Complete the following truth table for a 2 bits adder:

$t_1$	$B_1$	$B_0$	$A_1$	$A_0$	$t_1=s_2$	$s_1$	$s_0$
0	0	0	0	0			
0	0	0	0	1			
0	0	0	1	0			
0	0	0	1	1			
0	0	1	0	0			
0	0	1	0	1			
0	0	1	1	0			
0	0	1	1	1			
0	1	0	0	0			
0	1	0	0	1			
0	1	0	1	1			
0	1	1	0	0			
0	1	1	0	1			
0	1	1	1	0			
0	1	1	1	1			
1	0	0	0	0			
1	0	0	0	1			
1	0	0	1	0			
1	0	0	1	1			
1	0	1	0	0			
1	0	1	0	1			
1	0	1	1	0			
1	0	1	1	1			
1	1	0	0	0			
1	1	0	0	1			
1	1	0	1	0			
1	1	0	1	1			
1	1	1	0	0			
1	1	1	0	1			
1	1	1	1	0			
1	1	1	1	1			

**LAB no. 8.**

3. Realize the 2 bit ripple carry adder schematic using 1 bit full adders. Use the option „Create default symbol” to create a symbol for the full adder.



4. Simulate the ripple carry adder above and draw the waveforms on the grid below. Write down the delay times and the logic values on the waveforms.

